Modelling Parallelism With Circuits
What is Efficiently Parallelisable?

**Experience suggests:**
Some problems can be solved efficiently in parallel, while others can not.

How could this be shown?

**Intuitive definition:**
A problem has an efficient parallel algorithm if it can be solved for inputs of size $n$
- in polylogarithmic time, i.e., in time $O(\log^k n)$ for some $k \geq 0$,
- using a computer with a polynomial number of parallel processors, i.e., $O(n^d)$ processors for some $d \geq 0$. 

Note: Using $O(n^d)$ processors efficiently requires a massively parallel algorithm. However, one could always use fewer processors (each taking on more work), possibly leading to a proportional increase in time. The hard bit in parallelisation is to utilise many processors effectively – reducing to fewer processors is easy.
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Modelling Parallel Computation

What kind of “parallel computer” do we mean here?

1. How do processors communicate?
2. What can a processor do in one step?
3. How are processors synchronised?

Detailed answer: define **Parallel Random Access Machine (PRAM)**
Modelling Parallel Computation

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Detailed answer: define Parallel Random Access Machine (PRAM)

Our answer:
Details are not critical as long as we can make some general assumptions:

(1) Every processor can send a message to any other processor in $O(\log n)$ time
(2) In one step, each processors can perform one Boolean operation on “a few” bits, say $O(\log n)$
(3) Processor steps are synched with a global clock
Simple PRAM computations can be mapped to Boolean circuits (with some extra circuitry for executing more operations or for modelling message passing)

Circuits as models for parallel computation:
- circuit gates can operate in parallel – they only depend on their inputs
- the time needed to evaluate a circuit depends on its depth, not size (depth = longest distance from an input to an output node)
Example: Generalised AND

The function that tests if all inputs are 1 can be encoded by combining binary AND gates:

- size: $2n - 1$
- depth: $\log_2 n$

\[
x_1 \land x_2 \land x_3 \land x_4 \land \cdots \land x_5 \land \cdots \land x_n
\]
Small-Depth Circuits

Small depth = short (parallel) time

**However:** Every Boolean function can be computed by depth $O(\log n)$ circuits using $O(n2^n)$ gates (exercise)
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Hence, to capture “efficient parallel computation”, we also restrict the size:

**Definition 20.1:** For $k \geq 0$, we define $\text{NC}^k$ to be the class of all problems that can be solved by a circuit family $C = C_1, C_2, C_3, \ldots$ such that

- the depth of $C_n$ is bounded by $O(\log^k n)$, and
- there is some $d \geq 0$ so that the size of $C_n$ is bounded by $O(n^d)$
  (in other words: $\text{NC}^k \subseteq P_{/\text{poly}}$).

(NC is for “Nick’s class”, named in honour of Nicholas Pippenger, who studied such circuits, by Stephen Cook.)
Different complexity classes are obtained when allowing generalised Boolean gates with many inputs:

**Definition 20.2:** An AND gate with unbounded fan-in is a gate that computes a generalised AND function over an arbitrary number $n \geq 2$ of inputs. OR gates with unbounded fan-in are defined similarly.

For $k \geq 0$, we define $\text{AC}^k$ exactly like $\text{NC}^k$ but allowing circuits to use gates with unbounded fan-in.

**Example 20.3:** Generalised AND is in $\text{NC}^1$ and in $\text{AC}^0$. 
The NC Hierarchy

The classes $\text{NC}^k$ and $\text{AC}^k$ form a hierarchy:

- if $i \leq j$ then $\text{NC}^i \subseteq \text{NC}^j$ (obvious)
- if $i \leq j$ then $\text{AC}^i \subseteq \text{AC}^j$ (obvious)
- $\text{NC}^i \subseteq \text{AC}^i$ (obvious)
- $\text{AC}^i \subseteq \text{NC}^{i+1}$ (since generalised AND and OR can be replaced with $O(\log n)$ bounded fan-in gates as in our example)

Note: $\text{NC}^0$ is not a very useful class, as those circuits cannot process the whole input.
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The limit of this hierarchy is defined as $\text{NC} = \bigcup_{k \geq 0} \text{NC}^k$ so we get:

$$\text{AC}^0 \subseteq \text{NC}^1 \subseteq \text{AC}^1 \subseteq \cdot \cdot \cdot \subseteq \text{NC}^k \subseteq \text{AC}^k \subseteq \text{NC}^{k+1} \subseteq \cdot \cdot \cdot \text{ NC}$$

Note: $\text{NC}^0$ is not a very useful class, as those circuits cannot process the whole input.
Uniform vs. Non-uniform

Recall: a circuit family is uniform if it can be computed by a (restricted form of) Turing machine

- Our definitions of $\text{NC}^k$ and $\text{AC}^k$ do not require uniformity
- It is common to define uniform $\text{NC}^k$ and uniform $\text{AC}^k$ using logspace-uniformity (or even more restricted forms of uniformity)
- Clearly: uniform $\text{NC}^k \subseteq \text{NC}^k$ and uniform $\text{AC}^k \subseteq \text{AC}^k$

**Convention:** For the rest of this lecture, we restrict to (logspace) uniform versions of $\text{NC}^k$ and $\text{AC}^k$. 
Example: Parity is in $\text{NC}^1$
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However, we also have the following major result (without proof):

**Theorem 20.4 (see Arora/Barak, Chapter 14):** $\text{Parity}$ is not in $\text{AC}^0$, and therefore $\text{AC}^0 \not\subseteq \text{NC}^1$.
Example: FOL model checking

**FOL Model Checking**

- **Input:** First-order sentence $\varphi$; finite first-order structure $I$
- **Problem:** Is $\varphi$ satisfied by $I$?

We showed that this problem is PSpace-complete.
Example: FOL model checking

**FOL Model Checking**

Input: First-order sentence $\varphi$; finite first-order structure $I$
Problem: Is $\varphi$ satisfied by $I$?

We showed that this problem is PSpace-complete.
It turns out that this complexity is caused by the formula, not by the model:

**FOL Model Checking for $\varphi$**

Input: A finite first-order structure $I$.
Problem: Is $\varphi$ satisfied by $I$?

**Theorem 20.5** (see course Database Theory, Summer 2018, TU Dresden): For any first-order sentence $\varphi$, FOL Model Checking for $\varphi$ is in $\text{AC}^0$. 
Using the assumption of uniformity, we can solve circuit complexity problems by (1) computing the circuit and (2) evaluating it.

The following are not hard to show:

Theorem 20.6 (Sipser, Theorem 10.41): $\text{NC} \subseteq \text{P}$

Theorem 20.7 (Sipser, Theorem 10.39): $\text{NC}^1 \subseteq \text{L}$
Conversely, some known classes are also subsumed by NC:

**Theorem 20.8:** $\text{NL} \subseteq \text{AC}^1$

**Proof notes:**
General proof idea: (1) construct a “generalised” configuration graph for an NL machine (a graph that describes all possible configuration graphs for inputs of a given length, using transitions that depend on the actual input that is given); (2) check reachability of the goal state in this graph (basically by repeated matrix multiplication in the reachability matrix).

We do not give a proof here. Sipser (Theorem 10.40) sketches the proof for $\text{NL} \subseteq \text{NC}^2$; the proof for $\text{NL} \subseteq \text{AC}^1$ is the same but also uses that the depth is only logarithmic if we can use unbounded fan-in gates.
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We therefore obtain the following picture:

$$\text{AC}^0 \subset \text{NC}^1 \subset \text{L} \subset \text{NL} \subset \text{AC}^1 \subset \text{NC}^2 \subset \cdots \text{NC} \subset \text{P}$$
P-Completeness
NC defines a hierarchy of efficiently parallelisable problems in P

Are all problems in P efficiently parallelisable?
NC defines a hierarchy of efficiently parallelisable problems in $P$.

Are all problems in $P$ efficiently parallelisable?
Nobody knows.

State of the art:

- It is not known if $NC \neq P$ or not
- It is not even known if $NC^1 \neq PH$ or not
- It is clear that $AC^0 \neq P$ (since $AC^0 \subset NC^1$)
- It is clear that $NC \neq PSpace$ (exercise: why?)

“Most experts believe that” $NC \neq P$

$\implies$ if this is true, then some problems in $P$ cannot be parallelised efficiently.
Recall the definition from Lecture 11:

**Definition 11.7:** A problem $L \in P$ is complete for $P$ if every other language in $P$ is log-space reducible to $L$.

If $NC \neq P$ then P-complete problems are tractable but not efficiently parallelisable and therefore inherently serial.
Circuit Evaluation is P-complete

\[\textbf{Circuit Value}\]

<table>
<thead>
<tr>
<th>Input:</th>
<th>A Boolean Circuit (C) with one output, and an input word (w \in {0, 1}^n)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Problem:</td>
<td>Does (C) return 1 on this input?</td>
</tr>
</tbody>
</table>

**Theorem 20.9:** \textbf{Circuit Value} is P-complete.

**Proof:** Membership is easy. For completeness, we reduce the word problem of polynomially time-bounded Turing machines. A circuit for this problem was constructed in the previous lecture for Theorem 19.7. This circuit family is logspace-uniform (as already remarked in Theorem 19.13), so we get a logspace-reduction. \(\blacksquare\)
Propositional Horn Logic

A problem that is closer to artificial intelligence:

- A propositional fact is a formula consisting of a single propositional variable $X$
- A propositional Horn rule is a formula of the form $X_1 \land X_2 \rightarrow X_3$
- A propositional Horn theory is a set of propositional Horn rules and facts

The semantics of propositional Horn theories is defined as usual for propositional logic.

**Prop Horn Entailment**

Input: A propositional Horn theory $T$ and a propositional variable $X$

Problem: Does $T$ entail $X$ to be true?
Propositional Horn Logic is P-Complete

**Theorem 20.10:** Propositional Horn Entailment is P-complete.

**Proof sketch:** One can give a direct Turing machine encoding:

- We use propositional variables to represent configurations as for Cook-Levin
- We encode TM behaviour directly, e.g., for transitions \( \langle q, \sigma \rangle \rightarrow \langle q', \sigma', d \rangle \) we can use rules like \( Q_{q,t} \land P_{i,t} \land S_{i,\sigma,t} \rightarrow Q_{q',t+1} \land P_{i+d,t+1} \land S_{i,\sigma',t+1} \) (for all times \( t \) and positions \( i \))
- We do not need rules that forbid inconsistent configurations (two states at once etc.): Horn logic has a least model, and we don’t need to worry about other models when checking entailment
- Disjunctive acceptance conditions (“accepts if there is some time point at which is reaches an accepting state”) can be encoded by many implications (one for each case) without “real” disjunctions

For details, see Theorem 4.2 in Dantsin, Eiter, Gottlob, Voronkov: *Complexity and expressive power of logic programming (link)*. ACM Computing Surveys, 2001.
Horn logic is P-complete:
- One of the hardest problems in P
- Inherently non-parallelisable

However:
- Prop Horn Entailment can be decided in linear time
  [Dowling/Gallier, 1984]
- This does not imply that all problems in P have linear time algorithms
Summary and Outlook

Small-depth circuits can be used to model efficient parallel computation

 NC defines a hierarchy of problems below P:

\[ AC^0 \subset NC^1 \subset L \subset NL \subset AC^1 \subset NC^2 \subset \cdots \subset NC \subset P \]

P-complete problems, such as Horn logic entailment, are believed not to be efficiently parallelisable.

What’s next?

- Randomness
- Summary
- Examinations